Digital Pixel Sensor using Frame Averaging Unit for Fixed-Pattern Noise Correction and Pixel Size Reduction

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***Abstract*—Digital pixel sensors (DPS) have low-power, high dynamic range (HDR), and high-speed capabilities [1]-[8], suitable for applications requiring better performance over that provided by conventional CMOS image sensors. However, integrating an in-pixel analog-to-digital convertor (ADC) in a small pixel size leads to increased fixed-pattern noise (FPN) and degraded low-light performance. While noise reduction can be achieved through digital correlated double sampling (d-CDS) technique in DPS, the additional circuit and memory requirement increases the pixel size. In this work, a frame averaging unit (FAU) is developed to enable on-sensor FPN correction (FPNC) without increasing the pixel size. The developed approach achieves a 3.24-µm pixel size, delivering a temporal noise of 4.4 e^-_{rms} and an FPN of 2.4 e^-_{rms}.**

***Index Terms*—Digital pixel sensor (DPS), fixed-pattern noise (FPN), frame averaging unit (FAU).**

I. INTRODUCTION

In recent years, the demand of low-power and high-performance CMOS image sensors has enabled the surging development of DPS [1]-[8]. In [1]-[5], small pixel low-resolution DPSs are developed with low power consumption for wearables such augmented and mixed reality devices; in [6], a high speed DPS is reported to enable automotive or machine vision applications; in [7] and [8], high-speed high-resolution DPSs are implemented for professional photography purposes. Although DPSs offer high performances and global shutter, incorporating any noise reduction technique is difficult due to the limited area within the pixel. As a result, this leads to challenges of digital pixel noise or size reduction, impacting the low-light performance or preventing the implementation of small form factor DPS.

II. DIGITAL PIXEL SENSOR

In this work [1], a small digital pixel size of 3.24 µm is implemented in a 400×400 pixel array to enable lightweight wearable devices such as AR glasses. The digital pixel block diagram is shown in Fig. 1, including the CIS and ADC pixels connected through hybrid bond (HB). The CIS layer uses a 45-nm back-side illuminated (BSI) process and the ADC layer a 40-nm process. The CIS pixel is implemented based on a 5-transistor (5T) structure and the lateral overflow floating integration capacitor (LOFIC) technique [9] incorporating a dual-conversion gate (DCG) switch and a capacitor (C_S). Additionally, two high-density metal-in-metal (MIM) capacitors (C_{IN} and C_{INR}) are included to enable an AC-coupled A-to-D conversion [1]. The ADC pixel consists of a comparator, pixel control logics and a 10b 6-transistor (6T) SRAM.

In prior works [2]-[5], only 10b SRAM is used for storing the pixel data from each A-to-D conversion without additional noise correction, resulting in high FPN of 43.5 to 47 e^-_{rms}. On the other hand, although the d-CDS technique can be utilized to achieve good FPN performance, it requires additional control circuit and memory inside the pixel which prevents pixel size reduction. In [6] and [8], the pixel sizes are 4.95 and 5.94 µm with 22b and 30b in-pixel memory using advanced fabrication processes of 28 and 40 nm, respectively, to achieve good FPN performance. Although it is possible to realize d-CDS operation without adding additional in-pixel memory [7], it requires a very high-speed readout circuit to reduce the duration between the RST and SIG ADC operations. In addition, this high-speed readout circuit consumes significant pixel area, resulting in a pixel size of 6.9 µm using 65-nm process.

To achieve good noise performance without increasing the 3.24-µm pixel size in this work, an on-sensor FPN correction (FPNC) technique is developed. With a 3-layer stacked process, the on-sensor FPNC implementation is realized in the third (bottom) layer to minimize the sensor size. The FPNC is realized by implementing an FAU that generates reference frames for correction by the image signal processing (ISP) unit on sensor. With this approach, a good noise performance is achieved without increasing the pixel size. Additionally, this approach requires only a single A-to-D conversion compared to dual A-to-D conversions with d-CDS technique, resulting in reduced power consumption.

III. FRAME AVERAGING UNIT

The functionality of FAU is to generate reference frames representing the pixel intrinsic FPN which is stored in a frame buffer outside of the pixel array for correction by ISP. The FAU consists of an averaging algorithm to generate the reference frames using pseudo-dark frames from the pixel array. To generate the reference frames, the pixel array is configured to provide pseudo-dark frames by using a minimum exposure time and controlling the pixel transistors to isolate the FD from any photosignal arrival. During this process, the pseudo-dark frame is read out from the pixel array and sent to the FAU for processing. Since any frame readout contains both the temporal noise and FPN, multiple pseudo-dark frames may be averaged by the FAU averaging algorithm to minimize the temporal noise. Figure 2(a) shows the block diagram of reference frame generation using FAU with ISP disabled to reduce power consumption.

During sensor normal operation, the reference frame in the frame buffer is sent to ISP in parallel with the normal frame from the pixel array. Subsequently, the ISP subtracts the reference frame from the normal frame (pixel by pixel) to achieve FPNC, and dark pedestal adjustment and black-level correction are also performed at this stage if enabled. The block diagram of sensor normal operation using ISP is shown in Fig. 2(b). During this time, the FAU is disabled to achieve power savings.

Conventionally, FPN is sensitive to temperature change. To always ensure a consistent FPNC performance, the sensor is designed to support a reference frame rolling update operation. The rolling update operation can be triggered by a programmable duration (e.g. 60 seconds) or a temperature threshold (e.g. 5 degrees Celsius) between the current and the last (when reference frame was generated) temperature readings. This operation will use a new pseudo-dark frame and the existing reference frame to calculate a new reference frame, and it only occurs after the latest frame readout has completed and before the sensor enters the sleep state. Since the duration of rolling update is only 0.7 ms, the sensor normal operation is not interrupted. Additionally, the system can also manually trigger extra rolling update operation at the next frame if the updated reference frame does not meet the performance requirement. A complete sensor operation flow, including the FAU initialization, normal operation and rolling update, is shown in Fig. 3.

The FAU averaging algorithm is designed to use the existing reference frame and the latest pseudo-dark frame to generate a new reference frame. When a reference frame is not available (e.g. at sensor power-up), the first pseudo-dark frame is considered the new reference frame. The algorithm of reference frame generation can be written as

$$ReferenceFrame_{NEW} = round\left(\frac{A \times ReferenceFrame_{OLD} + B \times PseudoDarkFrame}{C}\right) \quad (1)$$

where $ReferenceFrame_{NEW}$ and $ReferenceFrame_{OLD}$ are the new and old reference frames, *PseudoDarkFrame* is the latest pseudo-dark frame from the pixel array, and *A*, *B* and *C* are configurable weightings dependent on the exact FAU operation mode and the desired performance. The rounding operation at the end of processing is chosen to minimize the circuit complexity and its power consumption without impacting the FPNC performance.

IV. EXPERIMENTAL RESULT

The sensor photomicrograph is shown in Fig. 4 with a small die size of 2.47×1.85 mm^2 thanks to the developed FPNC approach and FAU. The images in Fig. 5 are captured at dark condition to demonstrate the efficacy of the FPNC approach and the FAU averaging algorithm. The raw image of Fig. 5(a) has no correction and shows unacceptable noise due to the high FPN, which can degrade computer vision (CV) algorithm performance. The ISP corrected images of Fig. 5(b)-Fig. 5(e) demonstrate the improved noise performance with 1, 2, 4 and 8 pseudo-dark frames that are used during FAU initialization. The images show significant noise improvement once ISP is enabled and better noise performance with higher frame count during FAU initialization. The dark temporal noise and FPN are measured and shown in Fig. 5(f) and Fig. 5(g). The sensor achieves very similar temporal noise performance with and without FPNC at 4.4 e^-_{rms}, while achieving a significant FPN reduction from 10.7 e^-_{rms} to 2.4 e^-_{rms} with FPNC (8-frame FAU initialization). According to this result, the FPNC approach using the FAU is proved to be effective in reducing the FPN from the pixel array without increasing the temporal noise.

The virtually unaffected temporal noise after FPNC suggests that the implemented FAU averaging algorithm effectively removes the entire temporal noise from the image. However, it is not possible to achieve this result using only 8 pseudo-dark frames during FAU initialization, and the temporal noise is expected to increase slightly from 4.4 e^-_{rms} to 4.65 e^-_{rms} from theoretical calculation. One possible explanation to this result is that the sensor temporal noise is dominated by not only the white noise (such as the ADC read noise and SF thermal noise) but also the flicker noise (such as the SF and comparator input *1/f* noises). Nonetheless, the significantly reduced dark FPN helps improve the low-light performance dramatically and enables more accurate tracking and detection for CV applications. Additionally, the developed FPNC approach successfully enables the implementation of small digital pixel with good noise performance that meets the system requirements. The sample images under dark condition (5 lux) are shown in Fig. 6, and the image with ISP enabled shows significantly lower noise than that with ISP disabled.

Table 1 summarizes the noise performances of this work and prior work [1,2,4,6,7,8]. This work has achieved a small digital pixel size with only 10b in-pixel memory and low noise performance at the same time. A triple quantization (3Q) technique [2,3] is also implemented in this work, supporting 117-dB single-exposure high dynamic range (HDR) capture. The sensor has a figure of merit (FoM) of 0.0049 e^-_{rms}×pJ, significantly lower than other state-of-the-art DPSs.

V. CONCLUSION

A 3.24-µm DPS is developed for AR and smart glasses. The sensor has a 400×400 resolution and achieves a die size of 2.47×1.85 mm^2. To achieve good noise performance within a small pixel size, an on-sensor FPNC approach is developed with the FAU. The measured dark temporal noise and FPN are 4.4 and 2.4 e^-_{rms}, delivering good low-light performance.

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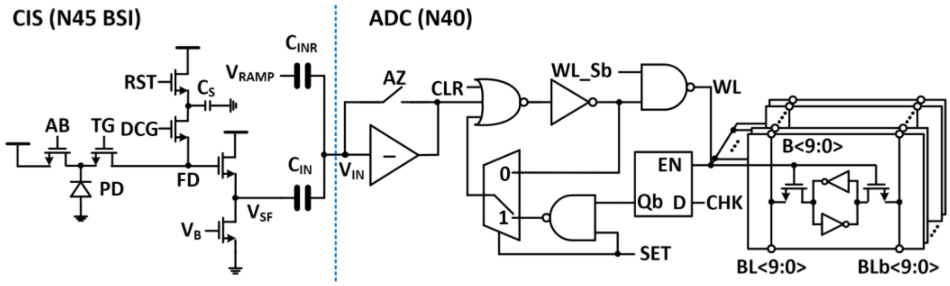
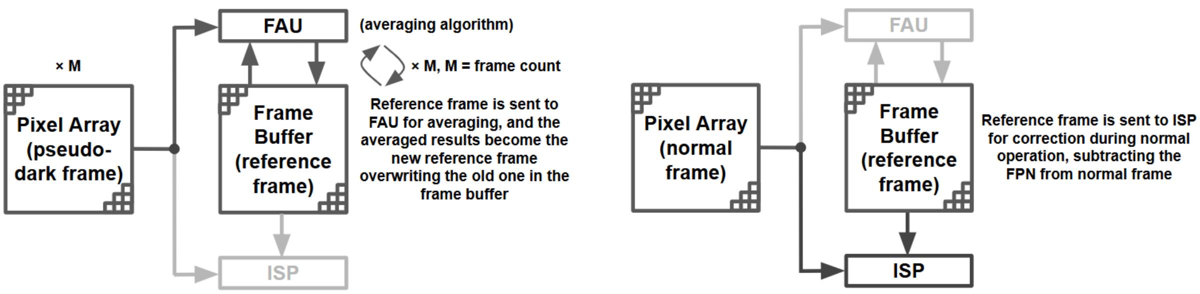


Fig. 1: DPS pixel block diagram.



(a) (b)

Fig. 2: Diagrams of (a) reference frame generation using FAU and (b) normal readout.

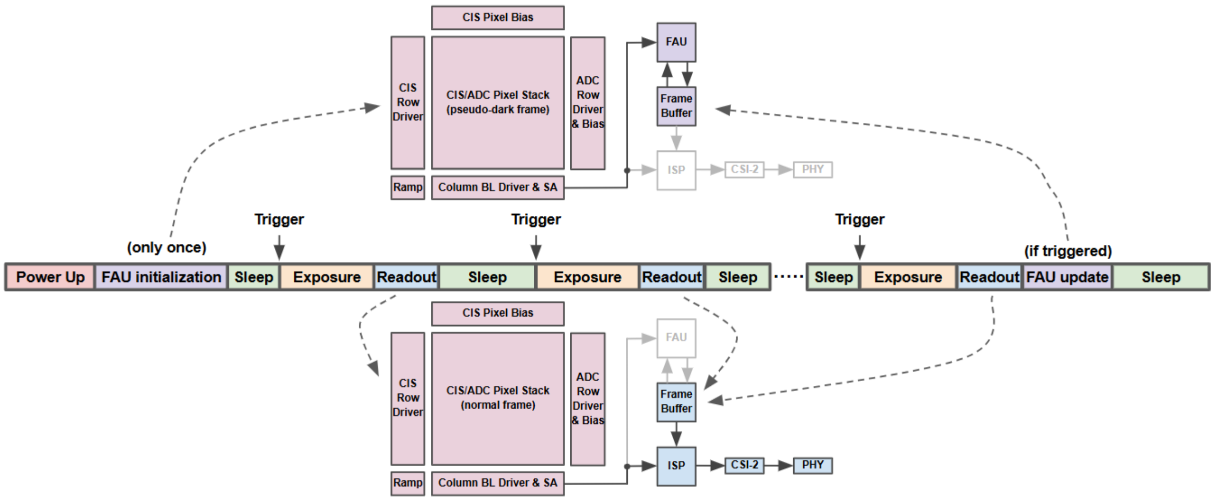
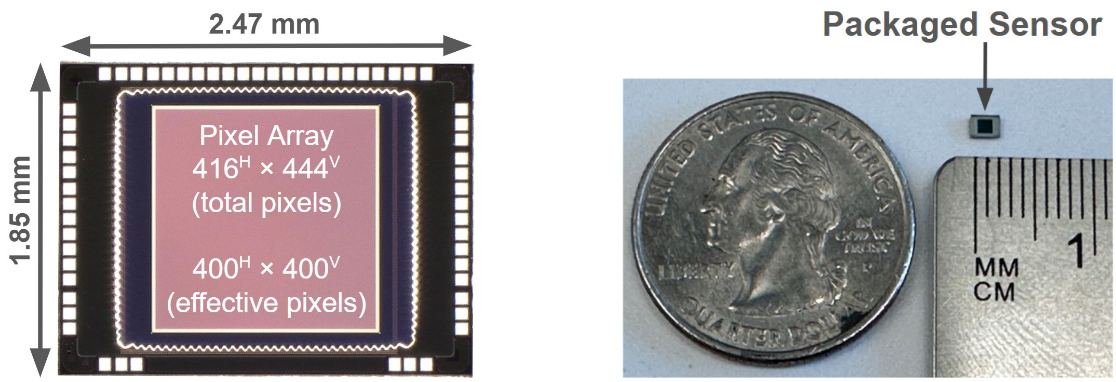
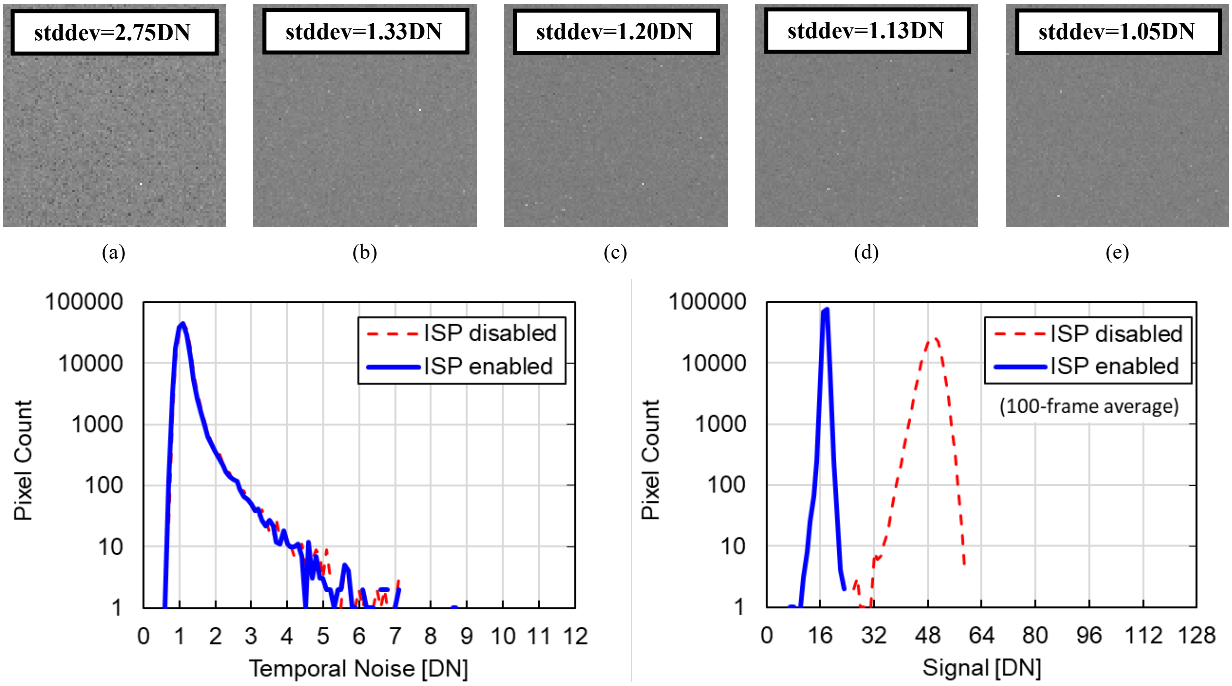


Fig. 3: Sensor operation flow.



(a) (b)

Fig. 4: (a) Sensor photomicrograph and (b) comparison with a U.S. quarter coin for scale.



(f) (g)

Fig. 5: Dark images with ISP (a) disabled, and enabled using (b) 1-, (c) 2-, (d) 4-, and (e) 8-frame averaging during FAU initialization. (f) Temporal noise and (g) FPN with ISP disabled (dashed line) and enabled using 8-frame FAU (solid line).

(a) (b)

Fig. 6: Contrast-enhanced images under 5-lux lighting condition. (a) Uncorrected. (b) Corrected with ISP and FAU.

Table 1: Performance summary.

	This work [1]	TED2022 [2]	JSSC2024 [4]	JSSC2022 [6]	JSSC2018 [7]	ISSCC2025 [8]
Pixel size [µm]	3.24	4.6	3.96	4.95	6.9	5.94
Process Node [nm]	45/40/40	45/65	45/40	65/28	90/65	90/40
Resolution (H×V)	400×400	512×512	640×640	1668×1364	1632×896	6144×4104
In-pixel memory	10b	10b	20b	22b	15b	30b
Dynamic Range [dB]	117	127	124	63.6	70.2	75.5
Noise floor [e^-_{rms}] @0dB	4.4	4.2	6.3	4.6	5.15	2.66
Dark FPN [e^-_{rms}] @0dB	2.4	47	43.5	1.94	0.58	0.26
Power [mW]	3.06@30fps	5.75@30fps	6.2@30fps	598.5@1200fps	746@660fps	1545@120fps
FoM* [e^-_{rms}×pJ]	0.0049	0.1809	0.097	0.78	1.24	0.2287

*FoM = (power × noise)/(number of pixels × frame rate × DRU); DRU = {(saturation/gain}/noise}.